ABSTRACT

In one exemplary embodiment, the disclosed VLIW processor comprises a number of threads where each thread includes a processing unit. For example, there can be two threads, where each of the two threads has its own processing unit. According to this exemplary embodiment, a number of VLIW packets are divided into a number of issue groups. As an example, two VLIW packets are divided into two issue groups each. The first issue group in the first VLIW packet is provided to a first thread for execution in the first thread processing unit during a first clock cycle. Concurrently, the first issue group in the second VLIW packet is provided to a second thread for execution in the second thread processing unit during the same clock cycle, i.e. during the first clock cycle. Moreover, the second issue group in the first VLIW packet is provided to the first thread for execution in the first thread processing unit during a second clock cycle. Concurrently, the second issue group in the second VLIW packet is provided to the second thread for execution in the second thread processing unit during the same clock cycle, i.e. during the second clock cycle. In this manner, various resources of the VLIW processor are efficiently utilized and two VLIW packets are executed during two clock cycles. As such, the processing speed of the VLIW processor is doubled without a significant increase in the power consumed by the VLIW processor.